Attorney's Docket No.: 07977/182002/US3413D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yamazaki, et al. Art Unit : 2823
Serial No.: 09/635,832 Examiner : Fernando Toledo
Filed : August 9, 2000
Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

Commissioner for Patents
Washington, D.C. 20231

REPLY TO NOTICE OF NON-COMPLIANT AMENDMENT

In response to the Notice dated March 20, 2002 in the above-identified application, please find below the entire amendment dated October 22, 2001 in its proper form as requested:



In the Claims:

Please elect Group II, claims 18-37 and 39-40.

Please amend claim 18-20, 23, 25, and 28-37 as follows:

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18. (Amended) An integrated circuit comprising:

a CMOS circuit;

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

April 2, 2002
Date of Deposit

S M Regan
Signature

Susan Regan
Typed or Printed Name of Person Signing Certificate